WHAT IS CLAIMED IS:

1. A fabrication method of a semiconductor device, comprising the steps of:

forming an interlayer dielectric film over an entire structure including a lower metal line formed over a semiconductor substrate;

forming on the interlayer dielectric film a barrier layer having an etching rate that is lower than an etching rate of the interlayer dielectric film, and selectively etching the barrier layer to expose a predetermined region of the interlayer dielectric film corresponding to where a via is to be formed;

forming a photoresist pattern on the barrier layer having an opening of a predetermined area corresponding to the exposed region of the interlayer dielectric film and to where a line opening is to be formed, the opening of the photoresist pattern having an area that is greater than an area of the exposed region of the interlayer dielectric film such that a region of the barrier layer adjacent to the exposed region of the interlayer dielectric film is exposed;

simultaneously forming the line opening and the via by etching the exposed regions of the barrier layer and the interlayer dielectric film dielectric film using the photosensitive film pattern as a mask; and

forming a metal plug by filling the line opening and the via with a metal material.

2. The fabrication method of claim 1, wherein the simultaneously forming the line opening and the via comprises, during etching the exposed regions of the interlayer dielectric film to form the via, first etching the exposed region of the barrier layer above the region where the line opening is to be

formed then directly etching the interlayer dielectric film to form the line opening to a depth less than a depth of the via.

3. The fabrication method of claim 1, wherein copper is the metal material.

4. The fabrication method of claim 2, wherein the forming a metal plug comprises depositing copper on the barrier layer and into the line opening and the via until filling the same, and performing chemical-mechanical polishing of the copper until the interlayer dielectric film is exposed.

5. The fabrication method of claim 1, wherein silicon carbide (SiC) is formed to a thickness of between 100 and 500Å to form the barrier layer.

6. The fabrication method of claim 1, wherein, prior to forming the interlayer dielectric film, a lower barrier layer is formed of a material having a lower etching rate than the interlayer dielectric film over all exposed elements including the lower line.

7. The fabrication method of claim 6, wherein silicon carbide (SiC) is formed to a thickness between 100 and 500Å to form the lower barrier layer.

8. The fabrication method of claim 6, wherein the simultaneously forming the line opening and the via comprises further etching the lower barrier layer following etching the exposed interlayer dielectric film to thereby form the via.

9. The fabrication method of claim 8, wherein over-etching by 5-15% is performed following the further etching the lower barrier layer to remove a predetermined region of the lower barrier layer.

10. The fabrication method of claim 1, wherein silicon oxy-carbide (SiOC) is formed to a thickness of between 10,000 and 14,000Å to form the interlayer dielectric film.

11. The fabrication method of claim 3, wherein, prior to forming the copper plug, a barrier metal layer is formed along inner walls of the line opening and the via, and on the barrier layer.

12. The fabrication method of claim 11, wherein the barrier metal layer is made of a material selected from the group consisting of Ti, Ta, and TaN.

13. The fabrication method of claim 11, wherein the barrier metal layer is formed to a thickness of 100~ 500Å .

14. The fabrication method of claim 3, wherein during formation of the copper plug, a first formation process is performed in which plasma chemical vapor deposition is used to deposit copper to a thickness of 500~ 1500Å , after which a second formation process is performed in which electroplating is used to deposit copper on the copper deposited in the first formation process and such that the via and the line opening are filled with copper.

15. The fabrication method of claim 1, wherein the lower line is made of one of copper and tungsten.